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(54) ELECTRONIC SWITCHING DEVICE

(71) We, SHARP KABUSHIKI KAISHA, formerly Hayakawa Denki Kogyo Kabushiki Kaisha, A Japanese company of, 22—22, Nagaike-cho, Abeno-ku, Osaka, Japan, do hereby declare the invention, for which we pray that a patent may be granted granted to us and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to a switching device for use in optoelectronics. GaAs negative resistance light emitting diodes (hereinafter referred to as GND) have a current control type negative resistivity and a light emission capability which increases with the current intensity, and the present invention provides a switching circuit in which the such GND can be incorporated.

Electro-photo conversion elements have been already developed such as the laser light-emitting diode etc. and their combination with photoelectric converters such as photo-diodes can constitute a circuit which operates using light as an information carrier. With such a circuit, however, there are required in preceding stages switching and amplifying devices for the control of light emittance. Thus, such known opto-electronics devices with their essential multitude of elements were inevitably highly complicated, this constituting a common limitation of such conventional devices. For having this limitation eliminated, efforts have been made by many researchers who envisaged development of an ideal element combining in it such diversified functions as switching, amplifying and light emittance but none of them could come up with any practice-proven solution before invention of GND.

The elements known before coming of GND invariably failed to emit light at room temperature and, although some of them could emit light at extremely low temperatures, their light emitting efficiency was so low that they could hardly qualify themselves for experimentation as circuit elements, i.e. elements built in circuits.

The present invention provides a switching device comprising a two-terminal semiconductor element having a voltage-current characteristic including a negative resistance region with a high impedance state and a low impedance state and having such light emitting characteristic that the light it emits increases with increasing intensity of the current flowing therethrough, impedance means connected in series with the semiconductor element, means for coupling into the series circuit an electrical source so as to supply current to the semiconductor element, means for switching the state of the semiconductor element and means for obtaining an output indicative of the state of the semiconductor element.

The present invention may employ the aforementioned GND, to provide a switching device of marked simplicity in circuit formation, whose capability was hitherto either unattainable or could only be matched by a far more complicated device of larger scale.

As is well known, the term switching device includes such circuits as NOT-, NOR-, NAND- and other logical circuits, flip-flop circuits and combinations thereof.

Within the present invention are switching devices which respond to a continuously changing series of light inputs or one-shot trigger light input or alternatively to a continuously changing series of electric inputs or one-shot trigger electric input.

The present invention enables provision for practical use of a switching device or a group thereof of outstanding simplicity for simul-

taneous on-off control of photo- and electric outputs.

Opto-electronics devices of the invention may have extremely high light emitting efficiency together with amplifying and switching functions, and may be well stabilized in operation at room temperature without calling for cooling means.

Switching devices in accordance with the invention can be made to respond as quickly as on the order of 10^{-7} sec. in terms of time lag.

Such switching devices, well stabilized in its operation, may also be non-wearing and ensure a semi-permanent service.

The invention is described further by way of example with reference to the accompanying drawings, in which:

Fig. 1 is a circuit diagram showing a switching device as a basic embodiment of the present invention.

Fig. 2 is a sketch showing the inside structure of the GND element incorporated in the circuit of Fig 1.

Fig. 3 is a characteristic curve showing the volt-ampere characteristic of the GND illustrated in Fig 2.

Fig. 4 is a characteristic curve showing the ampere-light output characteristic of the GND illustrated in Fig. 2.

Figs. 5 to 10 represent variations of the circuit shown in Fig. 1.

Figs. 11 to 13 are performance charts for the circuits of Figs. 5 to 10.

Figs. 14 and 15 are circuit diagrams showing applications of the circuit shown in Fig. 7.

Figs. 16 and 17 are circuit diagrams showing applications of the circuit shown in Fig. 1.

Fig. 18 is a circuit diagram showing a variation of the circuit of Fig. 1.

Fig. 19 is a performance chart for the circuit of Fig. 18.

Fig. 20 is a block diagram showing an application of the circuit of Fig. 18.

Fig. 21 is a timing chart for the circuit of Fig. 20.

Fig. 22 is a circuit diagram showing an application example of the circuit of Fig. 16.

Fig. 23 is the performance chart for the circuit of Fig. 21.

The switching device of Fig. 1 as a basic embodiment of the present invention comprises a two-terminal semiconductor unit 1 having current controlled negative resistivity which emits light output substantially proportional to input amperage, an impedance unit 2 connected in series with the aforementioned semiconductor unit 1 acting as a load thereon, a direct current power source 3 which supplies forward current to the said semiconductor, control means 5 for "changing" the mode of performance of the said semiconductor and means 6 for taking out output light or output electric signal or both from the abovementioned semiconductor unit or the series circuit including it.

The negative resistance light emitting diode GND 1 which, among others, forms the basis for the present invention is a PNPN element of 4-layer structure with GaAs as the principal ingredient, as illustrated in Fig. 2. The element is composed of N_1 106 as the base layer and successive layers mounted thereon, namely P_1 layer 105, N_2 layer 104 and P_2 layer 103. Between the successive layers are formed boundaries J_1, J_2 and J_3. Base layer N_1 106 and P_2 layer 103 are provided with metallic electrodes 107 and 102 respectively.

This GND 1 with its structure exhibits a current-control type negative resistance characteristic and is a diode of high luminous (i.e. light emitting) efficiency.

Figure 3 represents the volt-ampere characteristic of this PNPN diode and Fig. 4 the ampere-light output characteristic thereof.

When P_2 layer side is biassed positive and N_1 layer side negative, boundaries J_3 and J_1 are biassed forward but the intermediate boundary J_2 is biassed inversely. When the applied voltage is relatively low, the current is almost completely blocked, the element then behaving as suggested by domain I of the characteristic curve of Fig. 3.

As the bias voltage is increased, some of the electrons injected from N_1 region 106 reach boundary J_3, thus facilitating the injection of holes from the P_2 layer, while the holes injected from P_2 layer 103 reach boundary J_1 to enhance injection of electrons from N_1 region 106, and thus progressively larger numbers of electrons and holes are injected into base layers P_1 and N_2, this giving rise to the phenomenon called electron multiplication.

Meanwhile, at boundary J_2 where a high intensity electric field is formed because of the inverse bias voltage applied, the condition gives rise to "break down", this, in turn, resulting in electron multiplication due to electron avalanche.

As a result of such mutual "action" a multitude of electrons are accumulated in N_1 layer and a multitude of holes in P_1 layer and this condition gives rise to inclination toward forward biassing of boundary J_2 and with that the potential difference at boundary J_2 decreases gradually, this resulting in decrease of the potential difference between two terminals of P_2 region and N_1 region (see domain II of the curve of Fig. 3). Finally the potential at boundary J_2 comes to the state of equilibrium, this virtually providing a condition of free conductivity and permitting flow of high amperage current (see domain III of the curve of Fig. 3). The volt-ampere characteristic of this element in such condi-

tion of free passage is identical with that of an ordinary diode.

Referring to the mechanism of light emitting, which, as well known, is consequence of recombination, the described structure of the element according to the invention allows recombination of the electrons injected from N_1 region 106 with the holes injected from P_2 region 103 to take place at boundaries J_1 and J_3 and this it could easily be assumed that with the invented element light emittance can proceed more efficiently than with an ordinary light emitting diode.

As may be seen from Fig. 4, the light output of GND 1 is roughly proportionate to the input current intensity, this being true in all of domains I, II and III.

With current intensity as "I" and light output as "P", this relationship could be represented approximately by the formula

$$P \alpha I^n$$

wherein "n" is a constant characteristic of the given diode.

Described below is an example of the manufacturing method for the abovementioned GND.

With Si alone as impurity it is possible to have 3 PNP regions formed in one process on N-type base plate by a method called liquid phase growth process.

Atoms of Group IV such as Si, Ge, Sn are impurities which can act on GaAs as donor and also as acceptor and hence may be called bifunctional. Such Group IV atoms act as donors when they replace Ga atom, while they are acceptors when As atom is to be replaced.

As Si dope GaAs epitaxial layer is allowed to grow by the liquid phase growth process, n-type GaAs does grow at relatively high temperatures but at lower temperatures inversion from n- to p-type takes place in the course of growth. This n—p invertion temperature depends on such factors as the crystallization orientation of GaAs base plate, the type of doping agent etc. but by far the most important factor is the cooling rate in the course of growth. This knowledge may be utilized for preparation of an element of the desired structure. So, first p-type layer or region may be allowed to grow under cooling, then cooling rate may be enhanced to induce growth of n-type layer and then inversion may be allowed to take place for resultant growth of p-type layer, and thus 3 layers of types p-n-p can be allowed to grow successively by mere control of the cooling rate.

The Si dope GaAs negative resistance electric field light emitting diode GND thus prepared has a high quantum yield in light emittance of 2 to 3%, or up to 10 times that of a conventional diode and hence can well function at room temperature.

The threshold voltage, V_{th}, threshold amperage, I_{th}, holding voltage, V_h, and holding amperate, I_h, of the diode thus prepared are as follows:

V_{th}=2—25 volts I_{th}=0.1—20 mA
V_h =1.3—1.4 volts I_h =1—70 mA

The response speed of GND 1 is determined by the length of time required for the electrons and holes to pass through what represent the base regions of PNP and NPN transistors comprising the PNPN 4-layer structure. Since the layers representing the base layers, namely layers P_1 and N_2 are both as thin as several microns to 10-odd microns, the response speed (turn-on time) is normally 1—5 μsec or so and it is even possible to get one with response speed (turn-on time) of 0.1 μsec.

The circuit shown in Fig. 5 contains as control means 5 a combination of resistance (2-A) and Photosensitive diode 7 connected in parallel.

As seen from the curve of Fig. 11, the voltage of power source 3-A is to be set higher than the threshold voltage, V_{th}, of GND, while the resistivity value of resistance 2-A is so chosen that, with diode 7 not exposed to input light 8, the load characteristic curve runs as indicated by line A, i.e. so that GND operates in domain I.

In this case the primary operating point is represented by the intersection point of the two characteristic curves 19, the current intensity at this point being I_3. Then, as diode 7 is exposed to input light, it gives rise to phenomenon identical with that resulting from lowering of the resistivity value of resistance 2-A and the load characteristic curve is now shifted from line A to say line a, with resultant shift of the operating point from 19 to 20, the second point of operation.

Under this condition the current intensity is at a high value at I_2 and hence GND 1 exhibits a very strong light emittance.

With this circuit the increase of light input turns on light output, while light output is turned off on decrease of light input, and hence this circuit can be utilized as shaping circuit for light wave form.

Fig. 6 represents a variation of the circuit shown in Fig. 5, with diode 7 connected in series with resistance 2-B.

The load characteristic curve related to GND characteristic and voltage of power source, V, is to be so set as indicated on Fig. 12 by line B, when diode 7 is in the state of free passage. The operating point under this condition is indicated by point 21 in the domain III, and light output 6 is "on". With decrease of input light 18 the load's resistivity value increases substantially and the

load characteristic curve is then shifted to say line b_1 with resultant shift of the point of operation to 22 in domain I.

With this circuit light output is turned on with the increase of input light, while it is turned off with the decrease of input light and hence this circuit can be utilized as an optical logical circuit.

The circuit shown in Fig. 7 has as control means (5 in Fig. 1) a photosensitive diode 9 connected in forward sense in parallel with GND 1. Against the characteristic curve of GND 1 the voltage, V, of power source 3-B and the resistivity value of resistance 2-B are chosen as indicated in Fig. 12: with diode 9 scarcely conductive, the load characteristic curve is to stand as indicated, for instance, by line B and operating point 21 is in domain III. With increase of input light 10 applied to diode 9, the operating point shifts readily to domain I and output light is turned off, and this circuit is useful as an optical NOT logical circuit.

The circuit shown in Fig. 8 is a variation of that in Fig. 7, provided with a second direct current power source 11 in the loop formed by GND 1 and diode 9. Its polarity is so set that the current supplied by this second source is in the sense opposite to that from the first power source 3-B (to GND 1).

When the input light 10 is ignorably weak and diode 9 is inconductive, the second power source 11 is totally inactive. As input light 10 is applied to diode 9, however, the small loop is supplied with second current, I_2, from second power source 11. The stronger this second current, I_2, is, the closer approaches the load characteristic curve to the origin of coordinates, as indicated by light b_2, and thus the range of operation can easily be extended to reach domain I.

The circuits shown in Figs. 5 to 8, each thereof, represents a switching device which operates in response to continuously increasing or decreasing light input to produce definitely on-off controlled light output or, if need be, electric output.

The circuit shown in Fig. 9 has a control means photo diode 14 which responds to trigger light for setting 16 connected in parallel with resistance 2-C and another photo diode 15 which responds to trigger light for resetting 17 in parallel with GND 1, both of these photodiodes connected in forward sense.

Against the characteristic curve of GND 1 the voltage of power source 3-C is set at V_1 higher than V_{th}, and the resistivity value of resistance 2-C is so set that, when both photo diodes 14 and 15 are inconductive, the load characteristic curve stands as indicated, for instance, by line C on Fig. 13: there should then be two points of stabilization, namely 251 and 24. When, with the operating point at 251 in domain I, photo diode 14 receives input light for setting 16, it results in shifting of the operating point past threshold voltage, V_{th}, into domain III and this stable operating point 24 is maintained even after the setting input light 16 has gone off.

When resetting input light 17 is applied to photodiode 15, however, the operating point is shifted back, past holding voltage, V_h, to domain I, and remains there, the stable point of operation 251 maintained even after resetting input light 17 has gone off.

This circuit represents a kind of flip-flop circuit whose switching operation is synchronized with trigger light on-offs, and hence can be utilized as a memory unit.

With the circuit of Fig. 10 control is accomplished by application of electric trigger signal to terminal 13 over terminal 4 and condenser 12. Against the characteristic curve of GND 1, the voltage of power source 3-D is set either at V_1 about V_{th} or V_2 below V_{th} and the resistivity value of resistance 2-D is so set that the load characteristic curve stands as indicated, for instance by line C or D on Fig. 13: there should then be two points of stabilization, 251 or 252 and 24. When, with the operating point in domain I at 251 or 252, positive trigger signal 109 of crest value enough to displace the operating point beyond threshold voltage, V_{th}, the operating point shifts to another point of stabilization, 24 in domain III, whereas on application of negative trigger signal 110 of crest value enough to displace the operating point beyond holding voltage, V_h, the operating point is shifted back to domain I. The circuit is so designed that the point of operation is held stable at either point of stabilization even after discontinued application of trigger signal.

This circuit represents a kind of flip-flop circuit whose switching operation is synchronized with electric signal, and hence can be utilized as a memory unit.

The circuit shown in Fig. 14 represents an application of the circuit of Fig. 7, provided with a plurality of photo diodes 271, 272 . . . connected in parallel, each of which is provided with each one means for supplying input light 261, 262 . . . The voltage of power source 3-B and resistivity value of resistance 2-B are to be chosen in the same manner as described for the circuit of Fig. 7.

With this circuit GND 1 has its operating point in domain I when input light is applied to any one of the plurality of diodes 271, 272 . . . and the operating point is in domain III only when none of the diodes receives input light. This circuit is useful as optical NOR logical circuit.

Circuits having the same function as the abovementioned circuit can be obtained by providing the circuit of Fig. 6 or Fig. 8

with a plurality of photo diodes connected in parallel with GND 1.

It may be easily understood that an optical OR logical circuit could be developed by replacing photo diode 7 of the circuit of Fig. 5 with a plurality of photo diodes.

The circuit shown in Fig. 15 is another application of the circuit of Fig. 7, provided with a plurality of photodiodes connected in series 291, 292, 293, each of which is provided with each one means for supplying input light 281, 282 . . . 283. The voltage of power source 3-B and resistivity value of resistance 2-B for GND 1 are to be chosen in essentially the same manner as described for the circuit of Fig. 7 or Fig. 14.

With this circuit GND 1 has its operating point in domain I only when input light is applied to all of the diodes 291, 292 . . . 293 and the operating point is in domain III when only one of the diodes does not receive input light. This circuit is, therefore, useful as an optical NAND logical circuit.

Similarly the circuit of Fig. 6 or Fig. 8 can be converted into a NAND logical circuit by providing a plurality of photo-diodes connected in series.

It may be easily understood that an AND logical circuit could be developed by applying the same theory to the circuit of Fig. 5.

The circuit shown in Fig. 16 represents a combination by optical means of 2 sets of the basic circuit illustrated in Fig. 1 being useful as a flip-flop circuit. In this circuit GND 30, 31, load resistances connected in series therewith 32, 33, output taking-out means 45, 46 and control means 42, 43 correspond to GND 1, load resistance 2, output taking-out means 6 and control means 5 of Fig. 1.

Terminals 40, 41 are connected to the direct current power source. Photo diode 38 is connected over resistance 36 to point 34 in the first circuit, this photo diode receiving the light emitting output from the second circuit. Similarly photo diode 39 is connected over resistance 37 to point 35 in the second circuit, this photo diode receiving the light emitting output from the first circuit. As light donating-receiving means 109, 110 may be used either photocouplers or photosensitive means such as optical fibres.

When 2 sets of the circuit of either Fig. 7 or Fig. 8 are to be used in combination, photo diode 9 could be utilized as photo-diode 38 or 39 of the abovementioned combined circuit. As control means 42, 43 may be used either optical or electric means such as those shown in Figs. 5 to 10. It is also possible to use a second power source like the one in Fig. 8 . . . power source 11.

When GND 30 has its operating point in domain III and is emitting light, photo-transistor 39 is kept conductive and, GND 31 of the second circuit having its operating point in domain I, light emitting output is "off". (First state of stabilization).

When under this condition a positive trigger signal is applied to point 35 of the second circuit or the resistivity value of load resistance 33 is lowered substantially to cause shifting of the operating point of GND 31 from domain I to domain III, photo diode 38 is made conductive and GND 30 of the first circuit has its operating point shifted to domain I and this state is maintained. (Second state of stabilization).

This circuit represents a R-S type flip-flop circuit when control means 42, 43 are used as setting input means and resetting input means respectively.

The circuit shown in Fig. 17 is another flip-flop circuit representing a combination of 2 sets of the basic circuit in Fig. 1, characterized by the connection made by impedance.

As the figure shows, GND 30, load resistance 32, output taking-out means 45 and control means 42 constitute the first circuit, while the second circuit is composed of GND 31, load resistance 33, output taking-out means 46 and control means 43, these two circuits connected over resistance 44. Terminals 40, 41 are connected to a direct current power source.

When GND 31 of the second circuit has its operating point in domain I and is not emitting light, this may be assumed to represent a high resistance and then, assuming that the load resistance for GND 30 of the first circuit comprises resistance 32 connected in parallel with series-connected resistances 44, 33, it may be well understandable that the load characteristic curve will be as indicated by line B of Fig. 12. GND 30 of the first circuit then has its operating point in domain III and emits light intensively. (First state of stabilization).

When under this condition control means 42 or 43 is actuated to have the operating point of GND 31 of the second circuit shifted to domain III or that of GND 30 of the first circuit shifted to domain I, second state of stabilization is produced, for in this case the first and second circuits are symmetrical with each other.

In this second state of stabilization GND 31 is "in the state of" low impedance and since the voltage level at connecting point 35 is low, it may be well understandable that the load characteristic curve will be as indicated by line b_2 of Fig. 12.

The circuit shown in Fig. 18 is still another variation of the basic circuit of Fig. 1, representing addition of a new function to the circuit of Fig. 10. The voltage of power source 3-E is set somewhat lower than threshold voltage, V_{th}, of GND 1, while the resistivity value of load resistance 2-F is so set that the load characteristic curve is as indicated by line E of Fig. 19 when photo diode

47 connected in parallel therewith is inconductive and as indicated by line E when said photo diode is conductive. Photo diode 47 is provided with means 51 for feeding back the light emitting output from GND 1 and also with means 48 for receiving input light from outside the circuit. Positive and negative electric pulse signals are applied to terminal 50 connected to this circuit over condenser 49.

When photo diode 47 is inconductive, the operating point of GND 1 is where marked by point 55 on the graph of Fig. 19. Arrival of input light then shift the operating point from 55 to 54 but not into domain III. When under this condition a positive trigger signal is applied to terminal 50, however, the operating point is immediately shifted to point 54 in domain III and the photodiode receiving the light emitting output of GND 1 itself remains conductive.

This state is maintained even after vanishing of input light and the operating point is shifted back to domain I only when a negative pulse is applied to terminal 50 or power source is "cut".

Thus, this circuit operates accurately synchronized with electric trigger signal and hence can be utilized as a memory unit to memorize acceptance of photo signal. The memorized information can be read from light output and this reading does not cause erasing of the memorized information.

Fig. 20 presents a shift register composed of a plurality of concatenated sets of the circuit shown in Fig. 18.

Block boxes 181, 182, 183, 184, 185, 186 on the figure, each thereof, is identical with the circuit shown in Fig. 18, terminals 501, 502 . . . 506 correspond to terminal 50, light input means 481, 482 . . . 486 correspond to light input means 48 and light output means 521, 522 . . . 526 to light output means 52 of Fig. 18. Power source 3-E may be used in common for all circuits. Terminals 501, 503 . . . 505 are connected in common to No. 2 terminal 57, while terminals 502, 504 . . . 506 are connected in common to No. 1 terminal 56.

Fig. 21 is the time chart for this concatenated circuit.

Chart (a) shows the wave form of No. 1 synchronous signal (clock pulse series) applied to No. 1 terminal 56, while chart (b) shows the wave form of No. 2 synchronous signal (clock pulse series) applied to No. 2 terminal 57. These are both electric signals, negative trigger signal followed by positive trigger signal. The chart show that No. 1 clock pulse timing is not in agreement with that of No. 2 clock pulse series.

Chart (c), the waveform thereof, shows an example of the light signal fed to the first light input means 481. On arrival of clock pulse following arrival of input light, the first circuit 181 is switched on and emits output light (see chart (d)). At this moment the second circuit 182 without arrival of clock pulse is not switched on even if it receives input light, not until arrival of clock pulse 59. (See chart (e)).

Thus each set in Fig. 20 is successively switched on and off synchronous with the clock pulse series and hence this concatenated circuit is useful as "shift register".

With this circuit the clock pulses are arranged in two series (No. 1 and No. 2) and thus precluded is the danger of a single trigger input causing successive switching of a multitude of circuits even in the event of a long pulse interval. This arrangement also precludes the danger of donation-acceptance of information interfered with even where the switch-over time is long compared with the pulse interval.

The circuit shown in Fig. 22 represents an application of the flip-flop circuit of Fig. 16, its function being conversion of a digital "amount" fed in a counter into an optical analogue.

Each of the comprising circuits, No. 1 65, No. 2 66 . . . No. 7 67, is a flip-flop circuit as shown in Fig. 16 and the resistivity value of load resistance is set as follows:

R=(resistivity value of 70)=(resistivity value of 71)

$R/2$=(resistivity value of 72)=(resistivity value of 73)

$R/2^2$=(resistivity value of 72)=(resistivity value of 73)

$R/2^{n-1}$=(resistivity value of 74)=(resistivity value of 75)

Counter input light signal is fed over feeding means 76, 77 into photo diodes 78, 79 of the first circuit 65 so as to have this flip-flop circuit 65 switched over.

The logical output from No. 1 flip-flop circuit 65 is then fed by photosensitive means 84, 85 into photo diodes 84, 85 of No. 2 flip-flop circuit 66 so as to have carry conveyed to No. 2 circuit and as this procedure is repeated, n-digit counter (scale of two) is formed. The output from each flip-flop circuit is fed over light outlet means 83, 89 . . . 96 into photoelectric converter 101 and, if need be, can be utilized after conversion into electric signals.

Fig. 23 presents a chart indicating the operational characteristic of this circuit. The load characteristic curve for resistivity value "R" is indicated by line F and the current intensity of GND 80 is I_0 when the No. 1 flip-flop circuit is switched on.

Similarly, I_1 is the electric intensity of GND 86 when No. 2 circuit is "on" and, as seen from the chart, $I_1=2I_0$. Similarly, the resistivity value of each load resistance is to be

so adjusted that the relationships $I_2=2^2I_o$, $I_3=2^3I_o$ . . . are established.

The characteristics of GND's for individual flip-flop circuits need not be identical.

WHAT WE CLAIM IS:—

1. A switching device comprising a two-terminal semiconductor element having a voltage-current characteristic including a negative resistance region with a high impedance state and a low impedance state and having such light emitting characteristic that the light it emits increases with increasing intensity of the current flowing therethrough, impedance means connected in series with the semiconductor element, means for coupling into the series circuit an electrical source so as to supply current to the semiconductor element, means for switching the state of the semiconductor element, and means for obtaining an output indicative of the state of the semiconductor element.

2. A switching device according to claim 1, wherein said coupling means couples a power source into the series circuit so as to bias the semiconductor element in the forward sense.

3. A switching device according to claim 1 or claim 2, wherein the means for switching is control means adapted to feed a photo or electrical control pulse into the series circuit for effecting the switching.

4. A switching device according to any of claims 1—3, wherein the means of switching is control means coupled to the series circuit.

5. A switching device according to all of claims 1 to 4, in which said control means includes a photosensitive element connected in the forward sense to the power source and means for feeding a photo control signal into said photosensitive element for switching said state of said semiconductor element.

6. A switching device according to claim 5, in which said control means includes a plurality of photosensitive elements each provided with independent means for feeding a photosignal into them so as to function as a multi-input logical circuit.

7. A switching device according to all of claims 1 to 4, in which said control means includes means for feeding said control pulse in electrical form into which said semiconductor element is connected with said impedance means to switch said state of said semiconductor element.

8. A switching device according to claim 7 which is additionally provided with a photosensitive element connected in parallel with said impedance means and in the forward sense to said power source and with means for having part of the output light from said semiconductor element applied to said photosensitive element.

9. A switching device composed of a plurality of switching devices as defined in claim 8, connected to form a plurality of stages and provided with means for having said output light of one stage applied to said photosensitive element of next stage and thereby affecting multi-stage connection of said plurality of switching devices, means for mutual connection of the points where said semiconductor elements of odd stages are connected with said means for providing an impedance, first means for generating periodic electric pulses capable of affecting a change of state of said semiconductor elements applied to such point of connection, means for mutual connection of the points where said semiconductor elements of even stages are connected with said impedance means, second means for generating periodic electric pulses differing in timing from said first pulse means and capable of affecting a change of state of said semiconductor elements applied to such point of connection, whereby the function of an optical shift register is provided.

10. A switching device fabricated from two switching devices as defined in all of claims 1 to 4 and provided with resistor means inserted between the points where said semiconductor elements and said impedance means are connected, and thereby provided with the function of a flip-flop circuit.

11. A switching device according to claim 1, wherein the two-terminal semiconductor element has first and second terminals, said semiconductor element being of four-layer PNPN construction with three PN junctions, said impedance means being connected to said first terminal of said semiconductor element, means being provided for forward biasing the two outer PN junctions of said three PN junctions and for backward biasing the intermediate PN junction, said biasing means being connected between said impedance means and said second terminal of said element to form said series circuit and for supplying current to said semiconductor element in the forward sense, means for feeding a photo or electrical control pulse into said series circuit for switching said state of said semiconductor element, said control pulse having a sufficient magnitude to cause a large carrier accumulation cancelling said backward bias at said intermediate PN junction to switch said element from said high impedance to said low impedance state, said element when in said low impedance state emitting light, and means for obtaining an output pulse indicative of the state of said semiconductor element from said circuit.

12. A switching device according to claim 11, wherein said negative resistance region is of the current-controlled type and said impedance connected to said first terminal is a load resistor.

13. A switching device comprising two switching devices each according to all of claims 1, 2 and 4 and in each of which the

two-terminal semiconductor element has first and second terminals, said impedance means being connected to said first terminal of said semiconductor element, a direct current power source coupled between said impedance means and said second terminal to form said series circuit and for supplying current to said semiconductor element in the forward sense, said control means including a photosensitive element connected in the forward sense to said direct current power source and means for feeding a photo control signal into said photosensitive element for switching said state of said semiconductor element and means for obtaining an output from said circuit indicative of the state of said semiconductor element; and further comprising means for applying the light output from said semiconductor element of the first switching device to said photosensitive element of the second switching device and means for applying the output light from said semiconductor element of the second switching device to said photosensitive element of the first switching device, thereby providing the function of a flip-flop circuit.

14. A switching device comprising a plurality of sets of switching devices each according to all of claims 1, 2 and 4 and in each of which each two-terminal semiconductor element has first and second terminals, said impedance means being connected to said first terminal of said semiconductor element, a direct current power source coupled between said impedance means and said second terminal to form said series circuit and for supplying current to said semiconductor element in the forward sense, said control means including a photosensitive element connected in the forward sense to said direct current power source and means for feeding a photo control signal into said photosensitive element for switching said state of said semiconductor element and means for obtaining an output from said circuit indicative of the state of said semiconductor element, said sets of devices being connected to form a plurality of stages in which the impedance means in each set has a value in accordance with the weight of an analog signal to be converted, with means for feeding the output light from the set in one stage to said photosensitive elements of the set in the next stage and thus accomplishing multi-stage operation of said plural sets of switching devices by optical means and with means for collecting output light from individual stages and thereby provide the function of digital to analog conversion.

15. A switching device substantially as hereinbefore described with reference to any of the accompanying drawings.

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Sheet 1

FIG.1

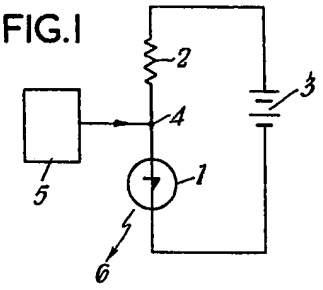

FIG.2

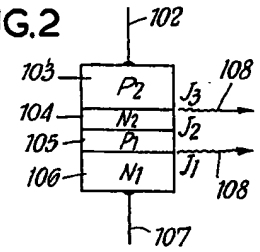

FIG.3

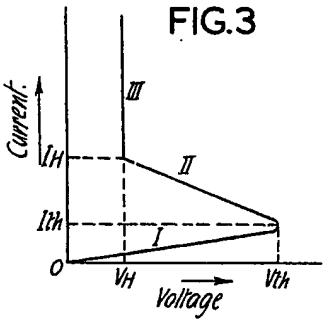

FIG.4

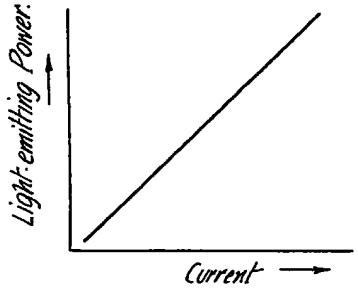

FIG.5

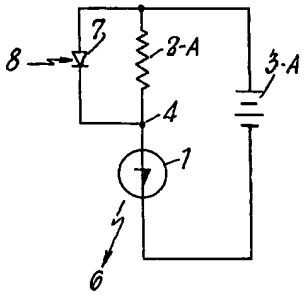

FIG.6

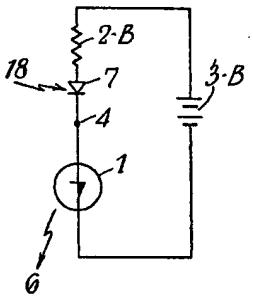

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FIG.7

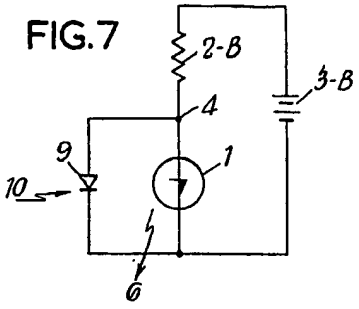
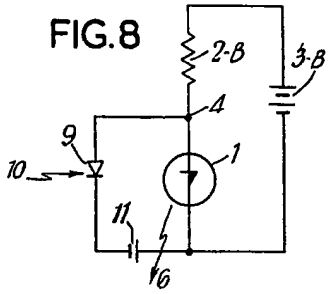


FIG.8



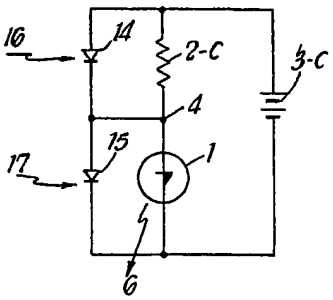


FIG.10

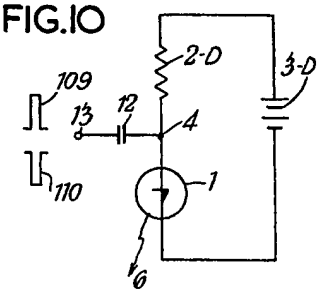


FIG.9

FIG.11

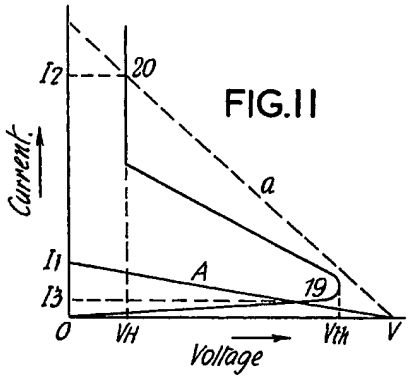


FIG.12

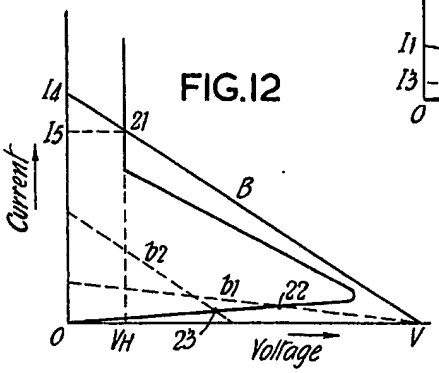


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FIG.13

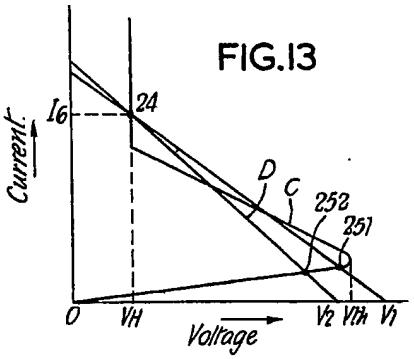

FIG.14

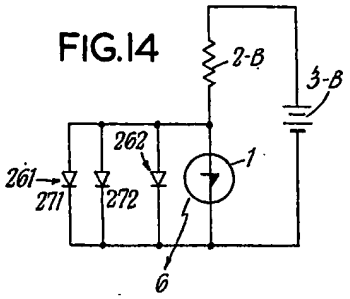

FIG.15

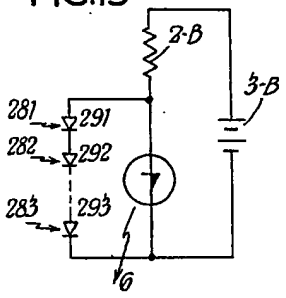

FIG.16

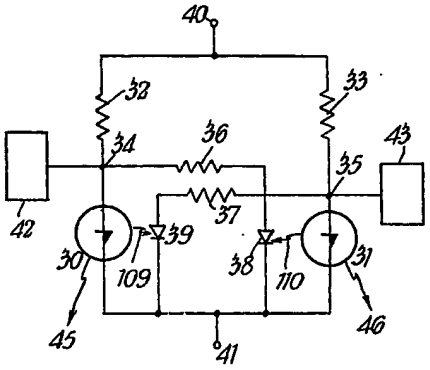

FIG.17

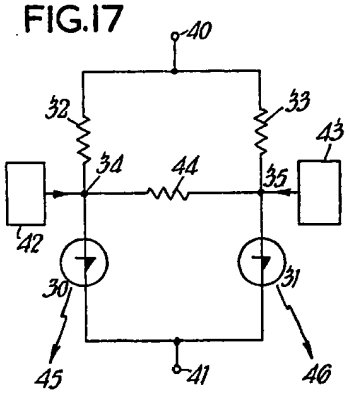

FIG.18

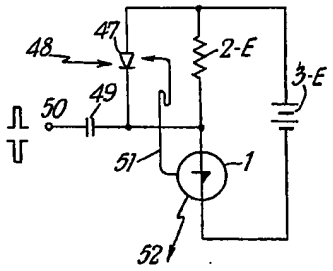

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FIG.19

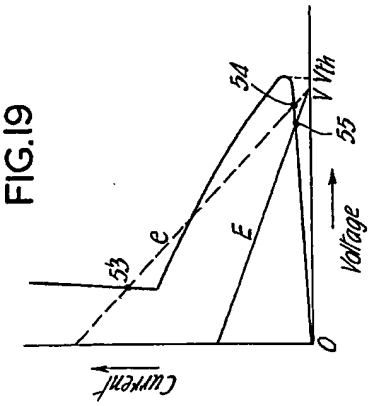


FIG.21

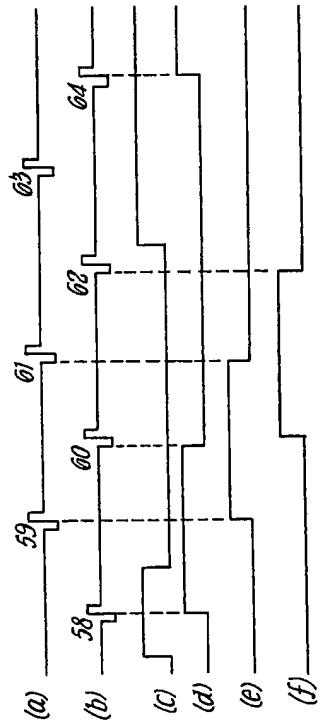
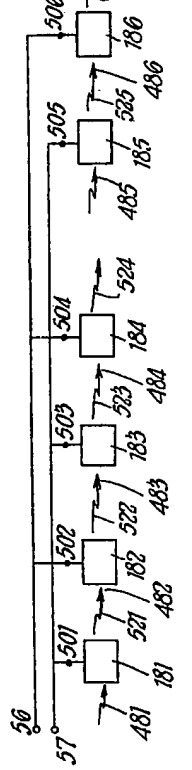


FIG.20



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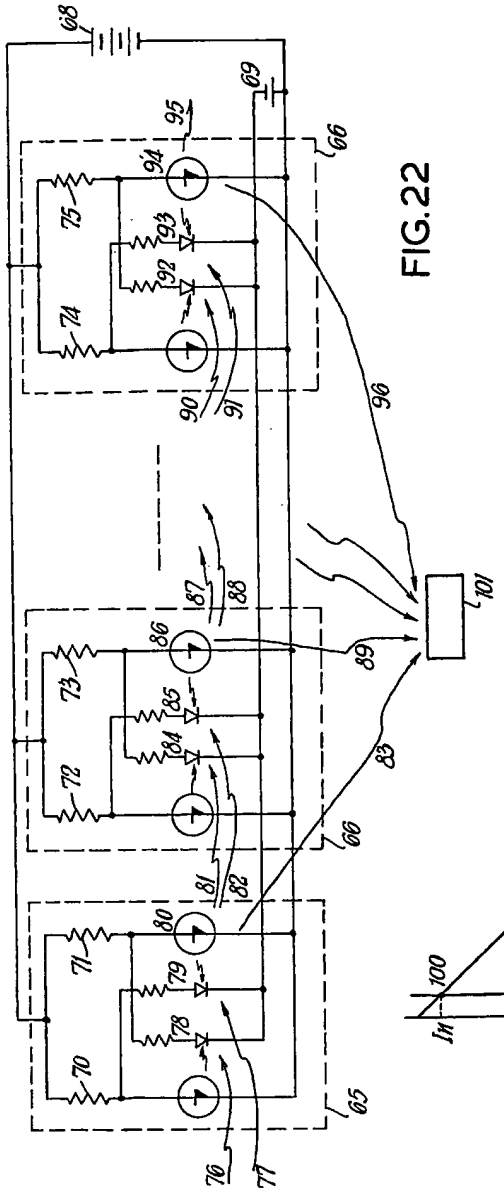

FIG.22

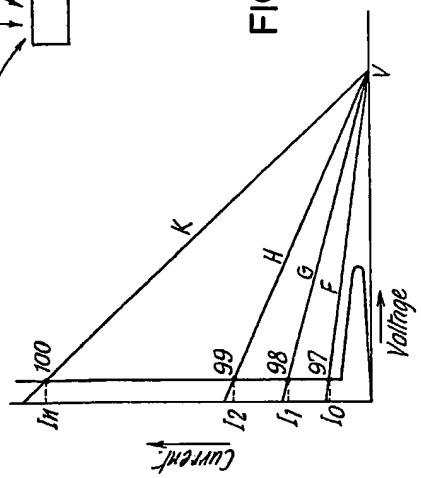

FIG.23